Fraunhofer IIS

Tage der Vertrauenswürdigen Elektronik 2025, Essen, 29. Oktober 2025

DI-Flowspace: Open-Source-Design-Kit für strahlungsharte Mikroelektronik in der Raumfahrt und Medizintechnik

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Open-Source Design Kit for Radiation Hardened ICs

Objective

Why do we care about Design Kits?

Process Design Kits **connect technology** development **with design** capability

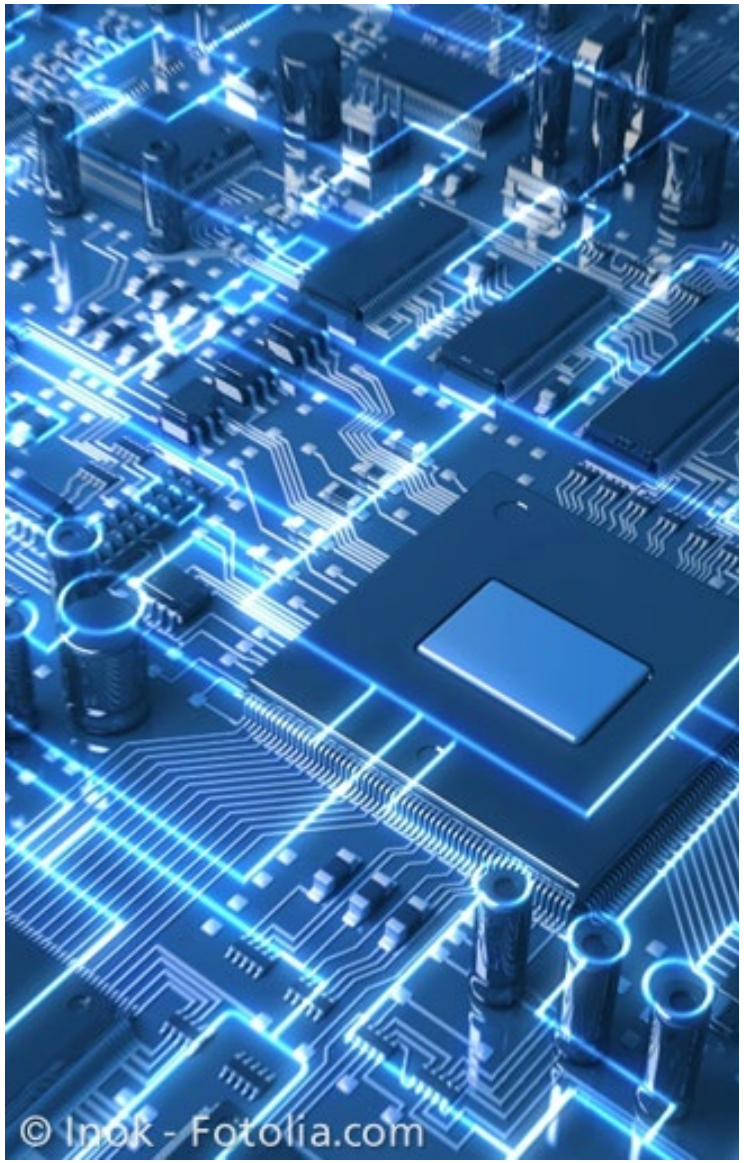
PDKs contain **available devices**, their **characteristics and limitations**

Designers utilize PDKs to **develop circuits** in the respective technology

Foundries **protect their technology IP** by restricting PDK access

This **prevents** Academia and SMEs from **using innovative technologies**

▶ **Open-Source Design Kits help leveraging innovative technologies for use in research and education**



Open-Source Design Kit for Radiation Hardened ICs

Objective

What do we aim for in the project?

Designers **need additional support** enabling them to utilize the technology

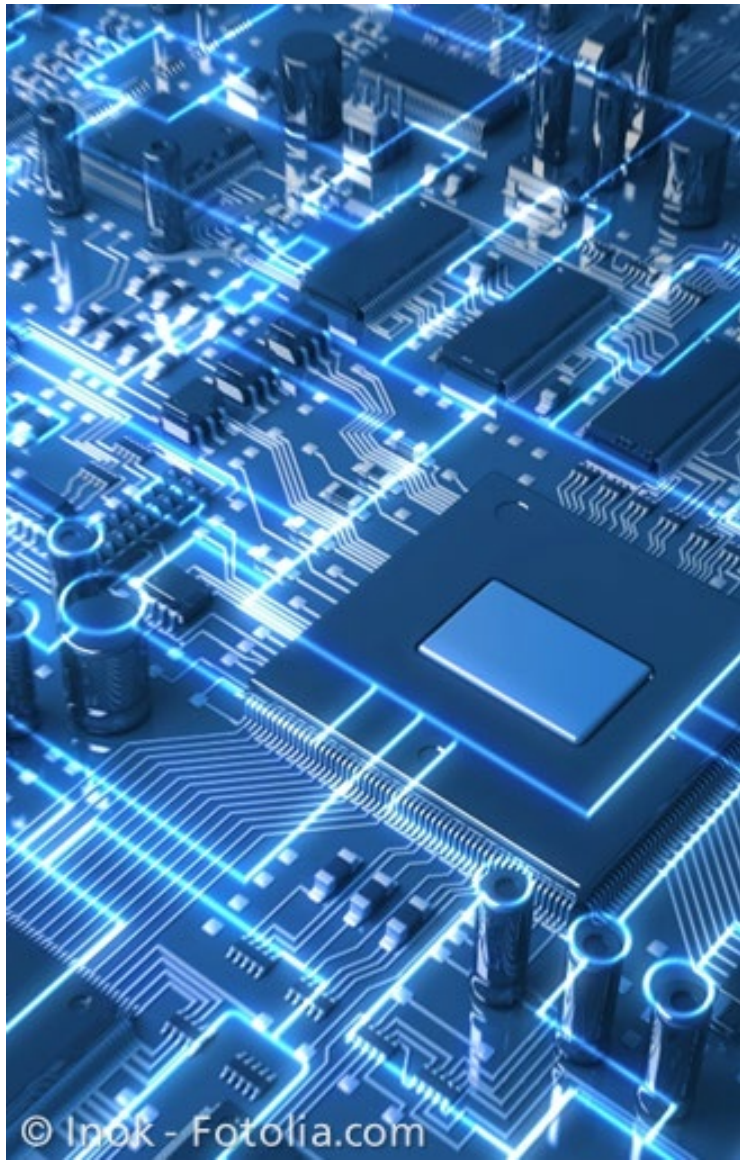
Specific **radiation hardened devices** and standard cells will be provided

Open-source tools are required that allow going through the **entire design process**

Add-on tools, i.e. for SRAM generation, **improve usability** of the design kit

Design quality will be ensured by additional CI/CD tools in the design flow

▶ **Additional Open-Source tooling will improve design capabilities and reduce risk of geopolitical dependencies**



Flowspace Project Status

Overview

Core Innovations

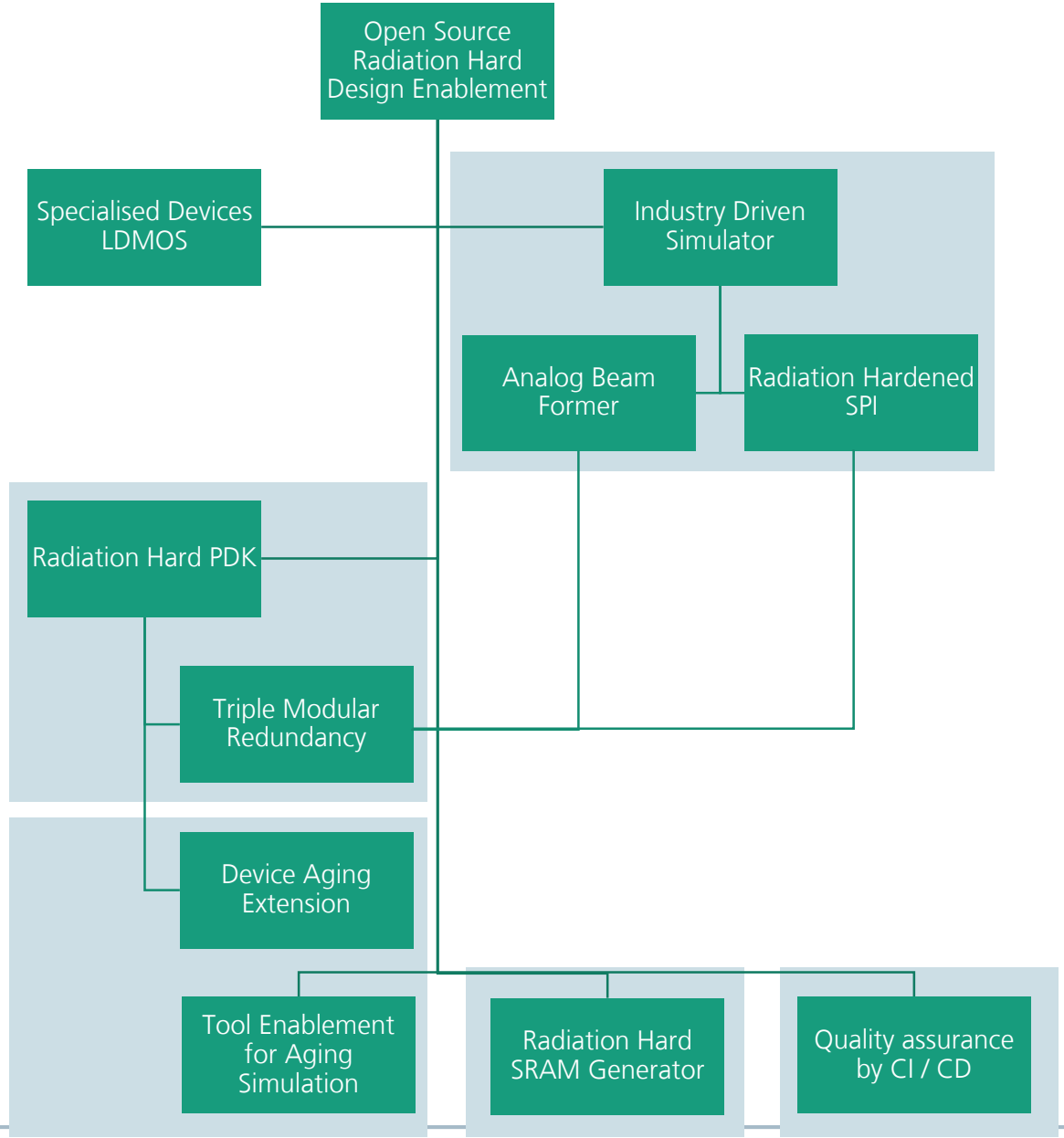
Open-Source European **Radiation Hard PDK**

Extended Radiation Hard **SRAM Generator**

Quality-Assured Development Flow by **CI/CD**

Added **Open-Source Simulator** Capabilities

Space-ready **analog beam former** with SPI



Flowspace Project Status

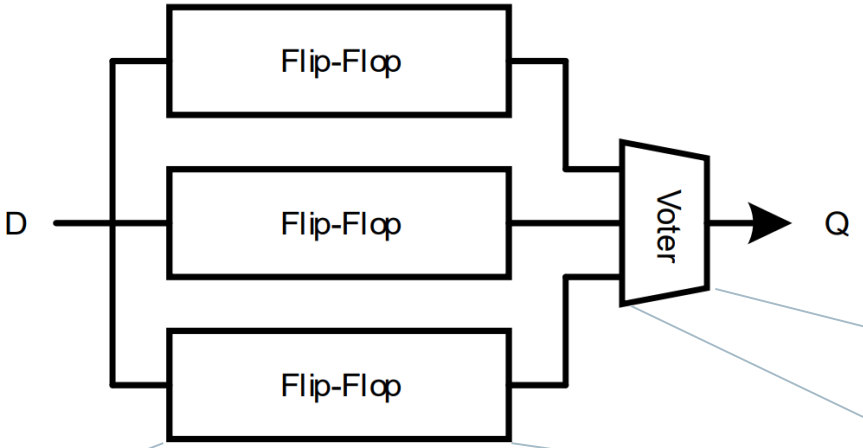
Radiation Hardened PDK

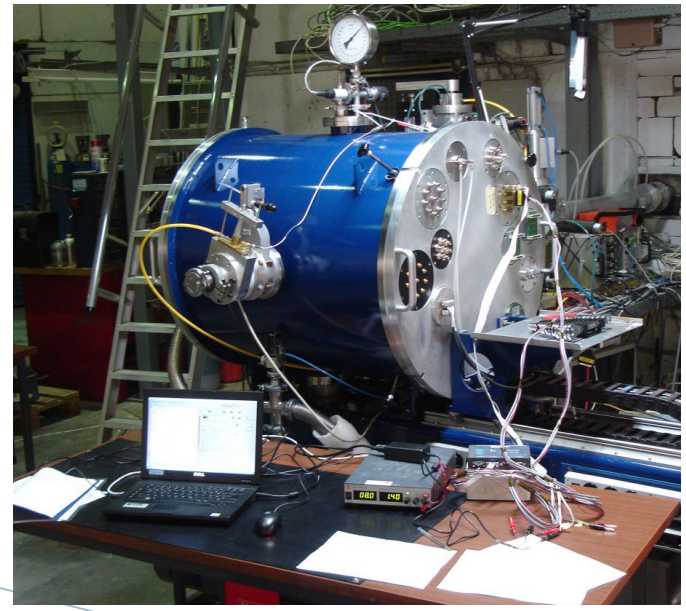
Triple Modular Redundancy Cells

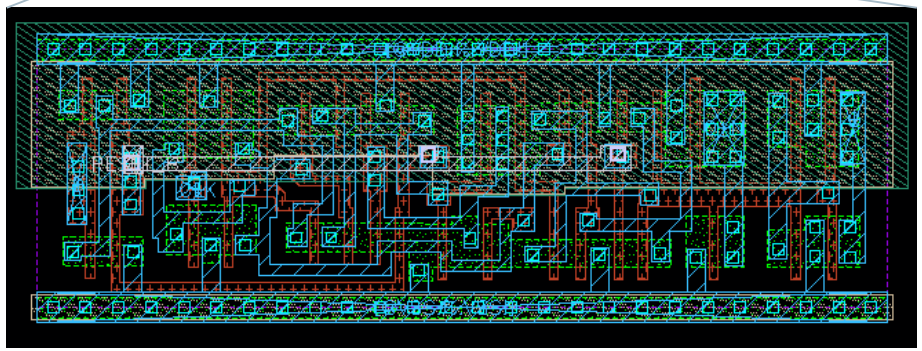
- Prevention of radiation induced Bit Flips
- IHP-Open130-G2 has limited # of cells
- Several TMR cells designed
  - Flip-Flop
  - Voter
  - Delay
  - SRAM blocks
- Test Chip Taped out April 2025
- Github release in Summer 2025
- Radiation tests being prepared

Aging Module

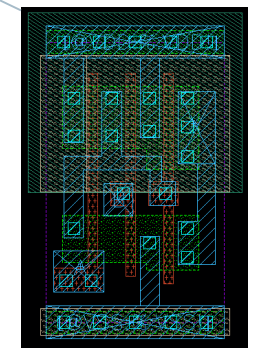
- First version under internal revision
- Github release in June



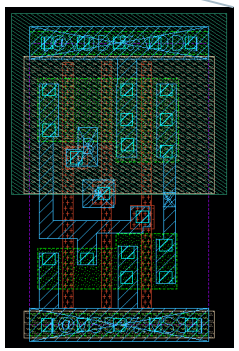




flip-flop cell



AND gate



OR gate

Flowspace Project Status

SRAM Generator

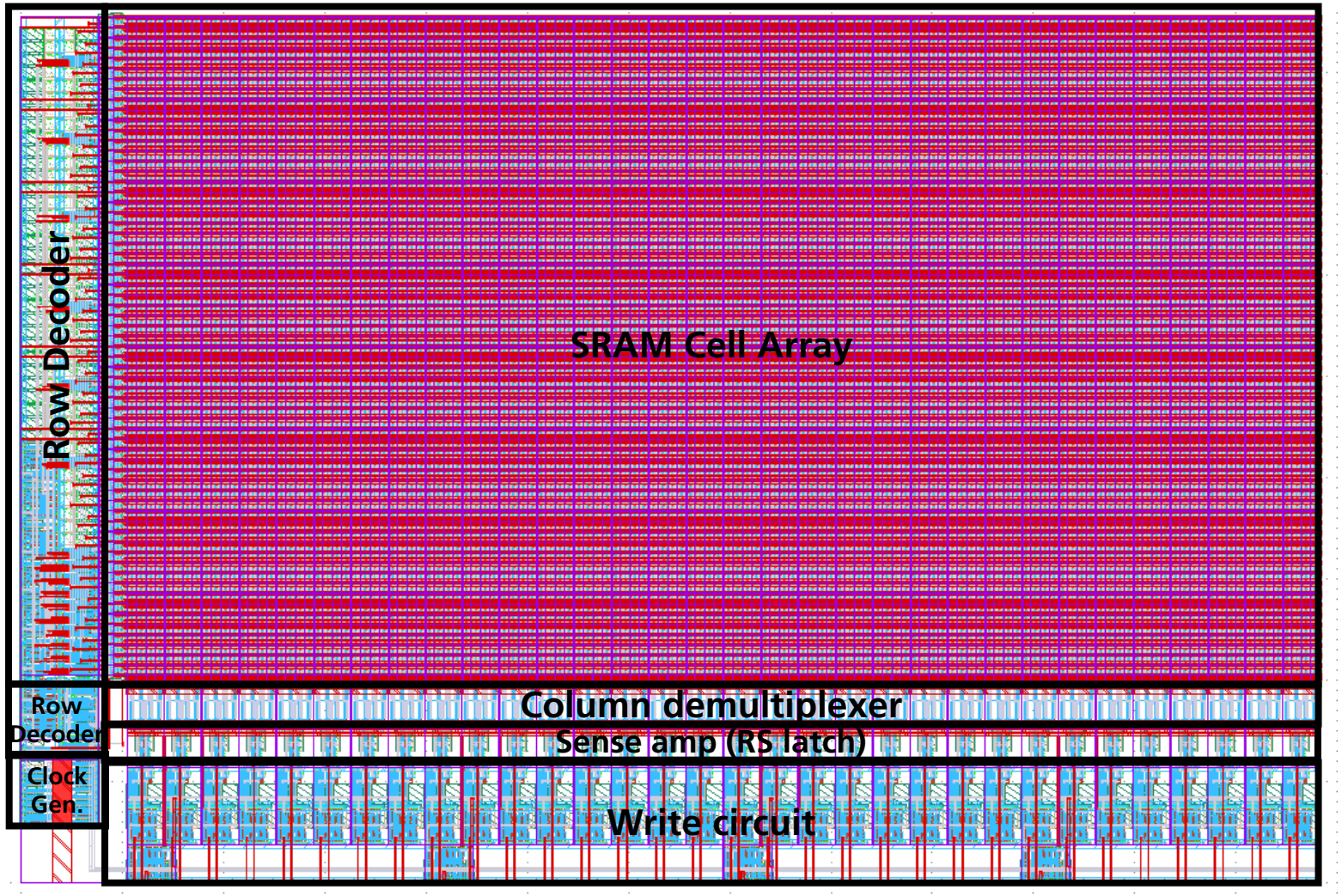
First single test structures

- Circuit and layout generation done
- Simulation based design optimization
- Single cells taped out in November

Next steps

- Design of larger arrays
- Analysis regarding timing
- Power analysis
- Functional test chip
- Radiation hardening
- Github release in the next weeks

Partnering with Chipflow



Flowspace Project Status

CI/CD System

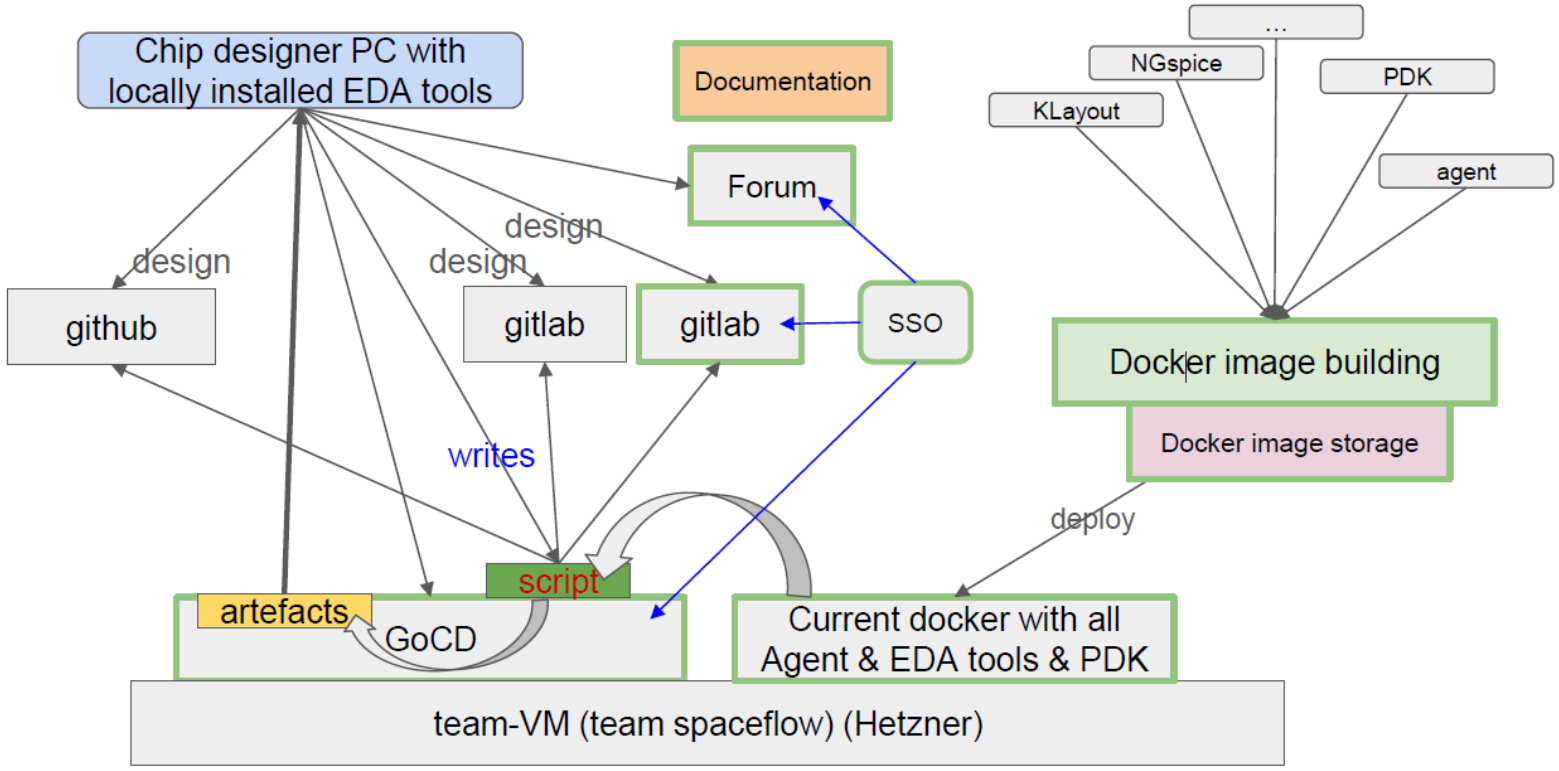
Integrity check of Design environment

- Tools
- PDK
- Golden Designs
- Available Open Source (can be hosted individually)
- Internal test on infrastructure started Q2/25

Docker

- focus on analog design
- development of own docker

Partnering with SymbioticEDA



Flowspace Project Status

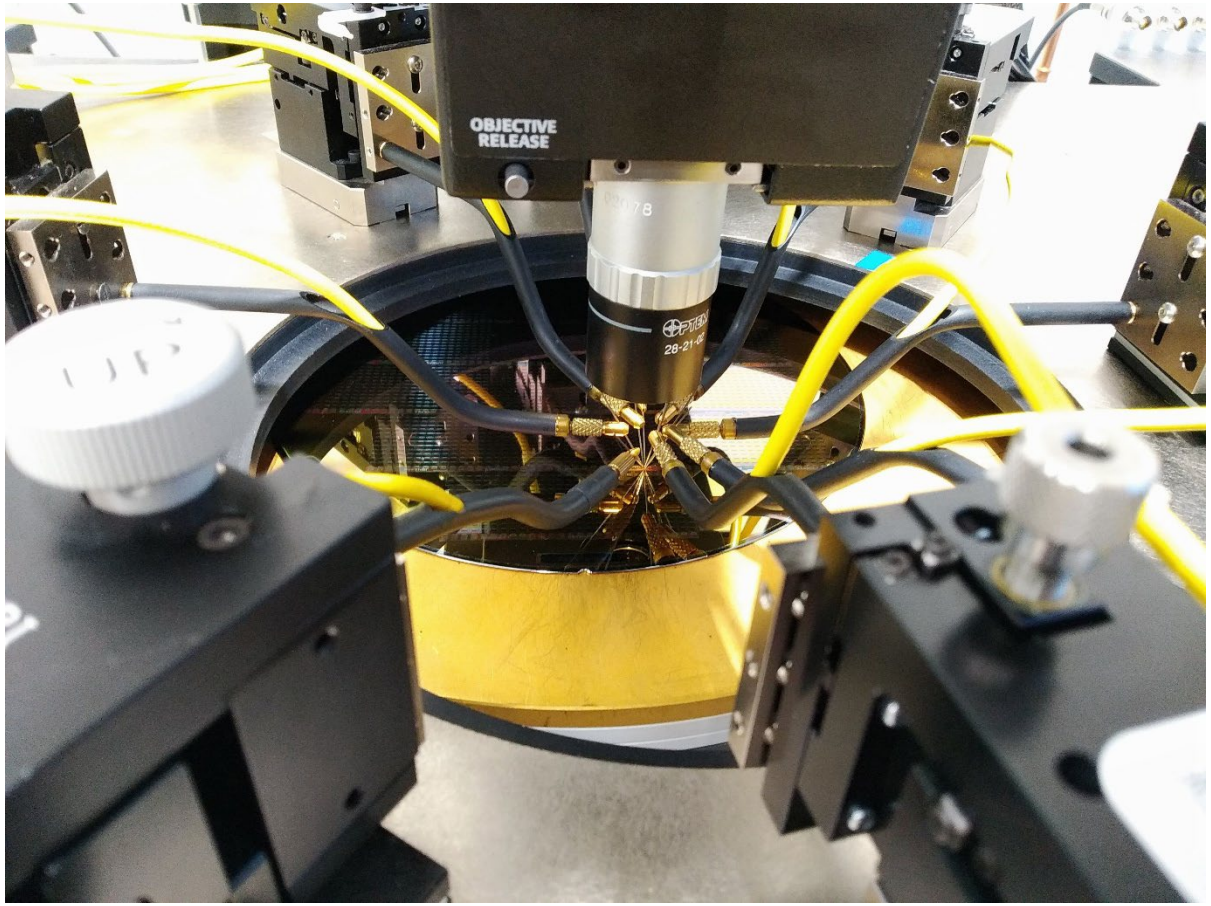
Open-Source Simulator Capabilities

Degradation measurements (aging mechanisms)
- Hot Carrier Injection (HCI)
- Negative Bias Temperature Instability (NBTI)

Creation of degradation models (aging)
- Extension of existing models for HCI
- Development of models for NBTI

Approaches for modeling the effects of radiation
- Total Ionizing Dose (TID)
- Single Event Upset (SEU)

Integration into the simulator ngspice
- Cooperation of Fraunhofer IIS with ngspice team from UDE



Open-Source Design Kit for Radiation Hardened ICs

Facts and Figures

Summary

Access to radiation hardened chip design and its handling

- Improved accessibility and ease of use for individuals, education and SMEs
- Understanding and application of radiation hardened technologies by open resources and tools

Strengthening the open-source community in chip design

- Advancement of an active open-source in analog, radiation hardened chip design
- Promotion of contributions and collaborative development by providing an integrated open tool flow

Partners

Academia

- **IHP – Leibniz Institute for High Performance Microelectronics**
- Fraunhofer Institute Integrated Circuits IIS
- University Duisburg-Essen

Industry

- IMST GmbH

Associated

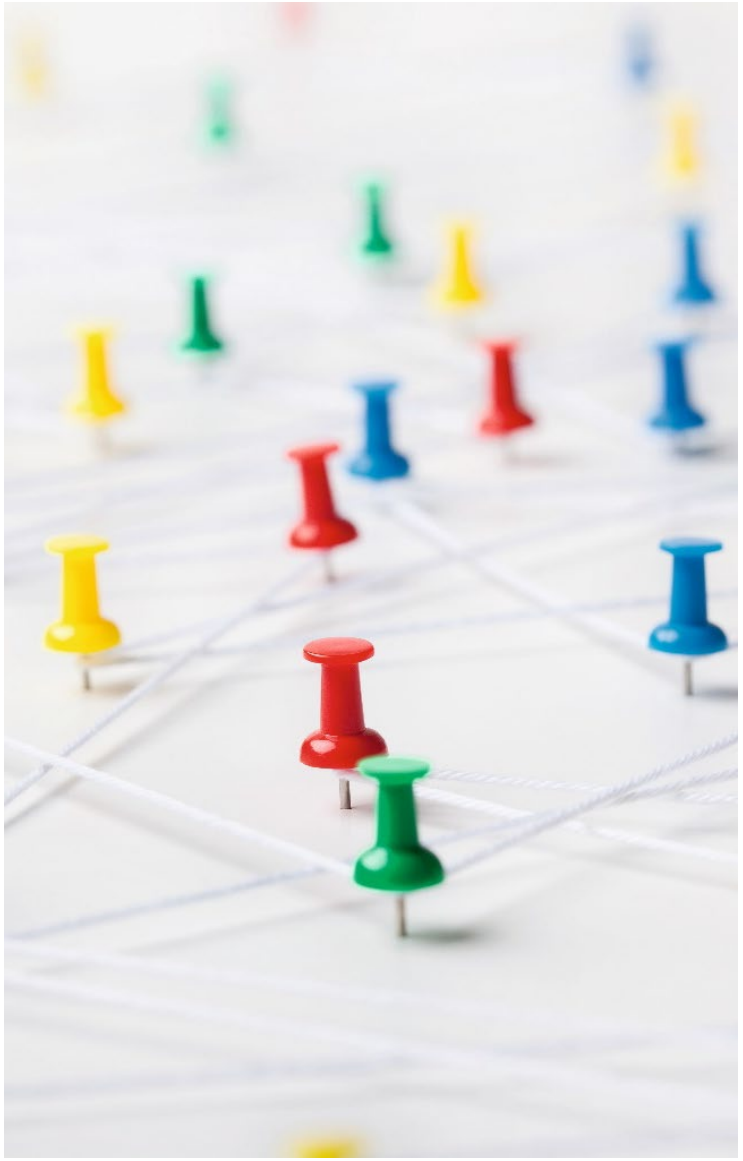
- SymbioticEDA
- Chipflow

Funding

2.443.110 €

GEFÖRDERT VOM

Bundesministerium für Forschung, Technologie und Raumfahrt



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Vielen Dank für Ihre Aufmerksamkeit

Fraunhofer IIS